Attorney Docket No.: 042390.P6942 *Patent*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Nardin et al.	)	Examiner: Craig, Dwin M.
	)	
Application No.: 09/475,717	)	Art Unit: 2123
	)	
Filed: December 30, 1999	)	
	)	
For: METHOD AND APPARATUS FOR FULLY AUTOMATED SIGNAL INTEGRITY ANALYSIS FOR DOMINO CIRCUITRY	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION PURSUANT TO 37 C.F.R. §1.131

Sir:

We, Mark D. Nardin, Hans Greub, and Sapumal Wijeratne, do hereby declare that:

1. We are the co-inventors of the above-captioned patent application and of the subject matter described and claimed therein.

2. Intel Corporation of Santa Clara, California, is the assignee of the patent application described above.

3. We are currently employed by Intel Corporation.

4. Prior to November 1, 1999, we jointly reduced to practice the invention as claimed in the above-captioned patent application (hereinafter "the present invention") in this country, as evidenced by Exhibits A, B, C, D, and E. All of these documents, in their unredacted form, were generated prior to November 1, 1999.

5. Exhibit A is a redacted Modification Log of software code, which practiced the present invention. The Modification Log shows that the present invention was reduced to practice prior to November 1, 1999. The last entry in the Modification Log was entered prior to November 1, 1999.

6. Exhibit B is a redacted portion of Parameter Extraction Code for extracting parameters of a set of domino logic circuits according to an embodiment of the present invention. The Parameter Extraction Code was reduced to practice prior to November 1, 1999.

7. Exhibit C is a redacted portion of an Output Log of software code that practiced the present invention. The Output Log was generated by the software code simulating a set of domino logic circuits prior to November 1, 1999.

8. Exhibit D is an unredacted Simulation Sequence File for simulating a set of domino logic circuits according to an ordered list. The Simulation Sequence File was generated by software code that practices the present invention prior to November 1, 1999.

9. Exhibit E is a redacted Simulation Time Stamp Log for a simulation executed on a set of domino logic circuits according to the Simulation Sequence File of Exhibit D. The Simulation Time Stamp Log was generated prior to November 1, 1999 by software code that practiced the present invention.

10. Evidence supporting that "extracting parameters of a set of domino logic circuits" was reduced to practice includes:

a. Exhibit B: This Exhibit illustrates a portion of Parameter Extraction Code for extracting parameters from domino logic circuits.

b. Exhibit C: This Exhibit of an Output Log implicitly provides evidence of extracting parameters of a set of domino logic circuits since the simulation which generated the Output Log could not have occurred without first extracting parameters of the set of domino logic circuits.

11. Evidence supporting that "simulating each domino logic circuit of a set of domino logic circuits" was reduced to practice includes:

a. Exhibit C, page 1, lines 31-35, 37-41, 45-50, etc.: These portions of Exhibit C illustrate the simulation results of domino logic circuits and therefore evidence that domino logic circuits were simulated.

12. Evidence supporting that "reporting results of the simulation indicating whether any of the domino logic circuit is likely to generate an erroneous output" was reduced to practice includes:

a. Exhibit C, page 2, lines 3 (for example): The portion "+0.048V DYNOUT" indicates that the particular domino circuit simulated has a positive noise margin

and therefore has a low likelihood to generate an erroneous output. A negative noise margin would be an indication that the particular domino circuit is likely to generate an erroneous output. The greater a negative noise margin the more likely an erroneous output. The more positive a noise margin the less likely an erroneous output.

b. Exhibit C, page 2, line 43: This portion of Exhibit C indicates that zero domino circuits of the simulated test circuit were likely to generate an erroneous output.

13. Evidence supporting that "scheduling a set of domino logic circuits into an ordered list, the ordered list positioning all domino logic circuits of the set of domino logic circuits feeding into an input of another domino logic circuit of the set of domino logic circuits before a position of the another domino logic circuit in the ordered list" was reduced to practice includes:

a. Exhibit D, page 1, lines 5, 13, 33, 43, and 50: The "simulation counts" schedule domino logic circuits into an ordered list or stages. This ordered list positions all domino logic circuits feeding into an input of another domino logic circuit before a position of the another domino logic circuit.

14. Evidence supporting that "simulating each domino logic circuit according to the ordered list" was reduced to practice includes:

a. Exhibit E: This Exhibit illustrates start and end time stamps of each stage of domino logic circuits scheduled for simulation in the Simulation Sequence File of Exhibit D. As can be seen the latest simulation end time of stage 1 "14:59:50" (Exhibit E, page 1, line 16) is before the earliest simulation start time of stage 3 "15:00:56" (Exhibit E, page 1, line 30). The latest simulation end time of stage 3 "15:47:53" (Exhibit E, page 1, line 40) is before the earliest simulation start time of stage 4 "15:49:02" (Exhibit E, page 1, line 50), and so on. Note, state 2 is not included in Exhibit E because stage 2 of the circuit under test did not include any logic circuits to simulate.

15. Evidence supporting that "determining whether any of the domino logic circuits is likely to generate an erroneous output" was reduced to practice includes:

a. Exhibit C, page 2, line 43: The indication that "0 domino circuits has negative noise margins" is a determination whether any of the domino logic circuits of the

circuit under test were likely to generate an erroneous output. Any domino logic circuit having a negative noise margin would have been likely to generate an erroneous output.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon.

Respectfully submitted,

Date April 15, 2004 _____

Mark D. Nardin

Date April 14, 2004 _____

Hans Greub

Date APRIL 14, 2004 _____

Sapumal Wijeratne